Tracking: Development Plans

Matthew Herndon
Johns Hopkins University

Tracking Meeting

Sep 24, 2003

Silicon Tracking Development Plans

Short Term Plans: 5.2.0

- Clean up crashes and uninitialized memory in ProductionExe(KalSiHit)
- Optimize TrackingKal code(compiler optimization)
- Update scripts for beamline production
- Convert SiExpected to use ChipOn table by default and test
- New user code: L00 routines and silicon layers hit accessors

Medium Term Plans: 5.3.0

- Simulation
  - New material description in the port card region - cables and tiled phantom layer
  - L00 in parameterized model
- User code for winter analysis
  - New material description in refit
  - Studies of silicon track errors: focus on stereo

- L00 optimized clustering cuts for resolution: Loose cuts in Production
- L00 final alignment
- L00 studies in dense physics environments

Long Term Plans: 7.x

- Standalone tracking
  - Improvements in forward efficiency: Already collected sets of high pt isolated tracks that fail Thanks to Phoenix electron code
  - Improvements in resolution and alignment: resolution considerably worse
- Phoenix muons - adapt electron code
- L00: Recover 20% missing efficiency: revisit excluded areas of the detector and the pedistal fit
- Use silicon to probe for residual alignment systematics in the COT
- Silimap integrator and fit: will improve speed and accuracy of fast track refit
- General program of code optimization for speed